Discrete-Time Modelling of an All-Digital Phased-Locked Loops for Clock-Generating Networks

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Abstract:
All-Digital Phase-Lock Loops (ADPLLs) are widely used for frequency synthesis in modern low-power electronics. They can be found in microprocessors, radio receivers, mobile telephones, GPS systems, etc. In the last two decades, the application of PLLs has expanded beyond the use of a single PLL and now includes PLL based networks. These networks serve for generating a distributed clock signal in microprocessors or in systems-on-a-chip (SoCs) where, due to complexity, it becomes impossible to supply a subsystem by a clock signal from a single crystal oscillator. Transistor-level modelling even of a single PLL is a time and resource consuming process. In order to understand the synchronisation of a PLL network and design such a networks, one requires a reliable model that can be simulated numerically and analysed analytically. In this work, we derive a mathematical model of an ADPLL employing a time- to-digital phase detector. The model we suggest represents a nonlinear discrete-time map and provides significant benefits for the simulation of a single PLL, a network of PLLs or their design. In particular, the model allows us to take into account the jitter of the reference and local clocks and other noises. The mathematical model (the map) is then compared with a behavioural model implemented in MATLAB Simulink and displays identical results. The simulation of the mathematical and behavioural models are further compared with experimental measurements.